The Course Structure for M.Tech (Digital Electronics & Communication systems) offered at Department of Electronics and Communication Engineering under autonomy system during the academic year 2012-13 is detailed below:

### M.Tech. 1st semester

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Code</th>
<th>Subject</th>
<th>T/P</th>
<th>Credits</th>
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<tbody>
<tr>
<td>1</td>
<td>ECEP1 1401</td>
<td>Advanced Digital Signal Processing</td>
<td>4</td>
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<td>2</td>
<td>MEP1 1401</td>
<td>Advanced optimization techniques</td>
<td>4</td>
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<td>3</td>
<td>ECEP1 1402</td>
<td>Digital System design</td>
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<td></td>
<td>Elective-1</td>
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<tr>
<td>4</td>
<td>ECEP1 1403</td>
<td>Detection &amp; Estimation of signals</td>
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<td></td>
<td>ECEP1 1404</td>
<td>Digital design through VERILOG</td>
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<td></td>
<td>ECEP1 1405</td>
<td>VLSI Technology &amp; Design</td>
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### M.Tech. 2nd semester

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<tr>
<td>1</td>
<td>ECEP1 1410</td>
<td>DSP Processors &amp; Architectures</td>
<td>4</td>
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<td>2</td>
<td>CSEP1 1413</td>
<td>Soft Computing techniques</td>
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<td>3</td>
<td>ECEP1 1411</td>
<td>Wireless communication &amp; Networks</td>
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<td>Elective-3</td>
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<td>ECEP1 1412</td>
<td>Analog &amp; Digital IC design</td>
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<td>ECEP1 1413</td>
<td>Radar Signal processing</td>
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<td>ECEP1 1414</td>
<td>Satellite communication systems</td>
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<td>Elective-4</td>
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<td>5</td>
<td>ECEP1 1415</td>
<td>Optical communication and Networks</td>
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<td>ECEP1 1416</td>
<td>System modeling &amp; simulation</td>
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<td>ECEP1 1417</td>
<td>VLSI Signal processing</td>
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<td>6</td>
<td>ECEP1 1209</td>
<td>HDL Programming laboratory</td>
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<td>7</td>
<td>GMRP 10206</td>
<td>Term Paper</td>
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### M.Tech. 3rd semester:

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<th>Credits</th>
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<tr>
<td>1</td>
<td>GMRP 20403</td>
<td>Internship</td>
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<td>2</td>
<td>GMRP 22005</td>
<td>Project work</td>
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### M.Tech. 4th semester

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<th>T/P</th>
<th>Credits</th>
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<td>1</td>
<td>GMRP 22005</td>
<td>Project work</td>
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</table>
M.TECH (DIGITAL ELECTRONICS AND COMMUNICATIONS SYSTEMS)

1st Semester

SYLLABUS

Course Title: ADVANCED DIGITAL SIGNAL PROCESSING
Course Code: ECEP1 1401

UNIT I  DISCRETE FOURIER TRANSFORMS: Properties of DFT, Linear Filtering methods based on the DFT, Overlap-save, Overlap -Add methods, frequency analysis of signals.

UNIT II  FAST FOURIER TRANSFORMS : Radix-2 FFT and Split- Radix FFT algorithms The Goertzel and Chirp Z transform algorithms

UNIT III  DESIGN OF IIR FILTERS: Design of IIR filters using Butterworth & Chebyshev approximations, frequency transformation techniques, structures for IIR systems –cascade, parallel, lattice & lattice-ladder structures.


UNIT V  MULTI RATE SIGNAL PROCESSING : Decimation by a factor D, Interpolation by a factor I ,Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion.

UNIT VI  POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Non-parametric methods :Bartlett ,Welch & Blackmann & Tukey methods.

UNIT VII  PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION: Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.


TEXTBOOKS

REFERENCES
M.TECH (DIGITAL ELECTRONICS AND COMMUNICATIONS SYSTEMS)

1st Semester

SYLLABUS

Course Title: ADVANCED OPTIMIZATION TECHNIQUES  
Course Code: MEP1 1401

UNIT – I LINEAR PROGRAMMING: Two-phase simplex method, Big-M method, duality, interpretation, applications.

UNIT – II ASSIGNMENT PROBLEM: Hungarian’s algorithm, Degeneracy, applications, unbalanced problems, traveling salesman problem.


UNIT – IV NUMERICAL METHODS FOR OPTIMIZATION: Nelder Mead’s Simplex search method, Gradient of a function, Steepest descent method, Newton’s method, types of penalty methods for handling constraints.

UNIT – V GENETIC ALGORITHM (GA): Differences and similarities between conventional and evolutionary algorithms, working principle, reproduction, crossover, mutation, termination criteria, different reproduction and crossover operators, GA for constrained optimization, draw backs of GA.

UNIT – VI GENETIC PROGRAMMING (GP): Principles of genetic programming, terminal sets, functional sets, differences between GA & GP, random population generation, solving differential equations using GP.


UNIT VIII Basic Problem solving using Genetic algorithm, Genetic Programming & Multi Objective GA and simple applications of optimization for engineering systems.

Text Books:
2. Optimization for Engineering Design – Kalyanmoy Deb, PHI Publishers
- 18 - Approved by BOS on 25th July 2009

References:
2. Genetic Programming- Koza MIT 1992
3. Multi objective Genetic algorithms - Kalyanmoy Deb, PHI Publishers
M.TECH (DIGITAL ELECTRONICS AND COMMUNICATIONS SYSTEMS)

1st Semester

SYLLABUS

Course Title: DIGITAL SYSTEM DESIGN  
Course Code: ECEP1 1402

UNIT – I DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT – II SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.


UNIT – IV TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.


UNIT – VI PROGRAMMING LOGIC ARRAYS: Design using PLA’s, PLA minimization and PLA folding.

UNIT – VII PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT – VIII ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

Text Books:

1. Z. Kohavi – “Switching & finite Automata Theory” (TMH)
2. N. N. Biswas – “Logic Design Theory” (PHI)

Reference Books:

2. Charles H. Roth Jr. – “Fundamentals of Logic Design”.
M.TECH (DIGITAL ELECTRONICS AND COMMUNICATIONS SYSTEMS)

1st Semester

SYLLABUS

Course Title: DIGITAL DESIGN THROUGH VERILOG (Elective-I)  Course Code: ECEP1 1404

UNIT – I  INTRODUCTION TO VERILOG : Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS : Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT – II  GATE LEVEL MODELING : Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flp flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.


if and if-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT – IV  MODELING AT DATA FLOW LEVEL : Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

SWITCH LEVEL MODELING.
Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

UNIT – V  SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES : Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises,

FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES : Introduction, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines)


UNIT – VII DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE LOGIC DEVICES: Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

UNIT – VIII  VERILOG MODELS: Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design, Design of Microcontroller CPU.
Text Books:


Reference Books:

M.TECH (DIGITAL ELECTRONICS AND COMMUNICATIONS SYSTEMS)
1st Semester

SYLLABUS

Course Title: CODING THEORY AND PRACTICE (Elective-II) Course Code: ECEP11406

UNIT-I INFORMATION THEORY: Entropy, Information rate, source coding: Shannon-Fano and Huffman coding techniques, Mutual Information, Channel capacity of Discrete Channel, Shannon-Hartley law, Trade-off between bandwidth and SNR.

UNIT II INTRODUCTION AND OVERVIEW ERROR CONTROL CODES: Examples of the use of error control codes, basic notions, coding gain. Characterization of Error control codes performance of error control codes, comparison of uncoded and coded systems.

UNIT III LINEAR BLOCK CODES: Linear block Codes and their properties, standard arrays, Syndromes, Weight Distribution. Error Detection/Correction Properties, Modified Linear block codes.

UNIT IV CYCLIC CODES: General theory, Shift Register Implementations, Shortened Cyclic codes, CRCs for Error Detection.


UNIT VI BCH and RS Codes: Algebraic Description, Frequency Domain Description, Decoding Algorithms for BCH and RS Codes.

UNIT VII CONVOLUTION CODES: Convolution encoders, structural properties of convolution codes, Trellis Diagrams, Viterbi Algorithm, Performance Analysis.

UNIT VIII Applications: Concatenated Codes, Interleavers, The Compact Disc, Codes for Magnetic recording.

Text Books:

Reference Books:
# M.TECH (DIGITAL ELECTRONICS AND COMMUNICATIONS SYSTEMS)

## 1st Semester

**SYLLABUS**

Course Title: ADVANCED SIGNAL PROCESSING LABORATORY  
Course Code: ECEP1 1218

<table>
<thead>
<tr>
<th>Expt No.</th>
<th>Experiment Name</th>
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<tbody>
<tr>
<td>1</td>
<td>Digital Circuits Design (Sub-System Level) Description using Verilog and VHDL</td>
</tr>
<tr>
<td>2</td>
<td>Verification of the Functionality of Designed Circuits using functional Simulator.</td>
</tr>
<tr>
<td>3</td>
<td>Timing simulation for critical path time calculation</td>
</tr>
<tr>
<td>4</td>
<td>Synthesis Reports of top-order designed Digital circuits</td>
</tr>
<tr>
<td>5</td>
<td>Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.</td>
</tr>
<tr>
<td>6</td>
<td>Implementation of Designed Digital Circuits using FPGA and CPLD devices</td>
</tr>
</tbody>
</table>