M. Tech (Digital Electronics & Communication systems)

COURSE STRUCTURE

Academic year 2013-14

M.Tech DECS 1st semester

<table>
<thead>
<tr>
<th>S.No</th>
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<th>Credits</th>
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<tbody>
<tr>
<td>1</td>
<td>ECEP1 1401</td>
<td>Advanced Digital Signal Processing</td>
<td>3+1*</td>
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<td>Advanced optimization techniques</td>
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<td>3</td>
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<tr>
<td>4</td>
<td>ECEP1 1403</td>
<td>Detection &amp; Estimation of signals</td>
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<td>5</td>
<td>ECEP1 1404</td>
<td>Digital design through VERILOG</td>
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<td>5</td>
<td>ECEP1 1406</td>
<td>Coding theory &amp; Practice</td>
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<td>6</td>
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<td>7</td>
<td>GMRP 10206</td>
<td>Term-paper</td>
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| Total | 20 | 03 | 24 |
### M.Tech DECS 2nd semester

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<td>ECEP1 1410</td>
<td>DSP Processors &amp; Architectures</td>
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<td>Soft Computing techniques</td>
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<td>Wireless communication &amp; Networks</td>
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<td>ECEP1 1414</td>
<td>Satellite communication systems</td>
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### Elective-IV

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### M.Tech DECS 3rd semester:

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### M.Tech DECS 4th semester

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*Tutorial
M.Tech (Digital Electronics and Communication Systems)
1st semester
A Y -2013-14

SYLLABUS

Course Title: ADVANCED DIGITAL SIGNAL PROCESSING      Course Code: ECEP1 1401

L    T    P   C
3     1  0    4

Course objectives:
Students undergoing this course are expected to:

- Analyzing Methods for frequency analysis of the signal using DFT
- Developing algorithms for Fast Fourier & Z Transform
- Designing of IIR filters using different techniques & strictures.
- Designing of FIR filters using different approximations & methods.
- Understanding the Sampling rate conversion methods
- Know finite word length effects in DSP systems
- Explore non-parametric methods for power spectrum estimation.
- Analyzing power spectrum estimation using parametric methods.

Course outcomes

After undergoing the course, students will be able to

- Apply the Methods for frequency analysis of the signal using DFT
- Analyze the frequency spectrum of the discrete time signal using FFT and Z-transform
- Apply the IIR filter for adaptive signal processing
- Implement the FIR filters for the noise reduction.
- Generate different signals at different sample rates
- Analyze and estimate the finite word length effects in DSP systems
- Estimate power spectrum using the non-parametric methods
- Apply the parametric methods for the estimation of power spectrum
UNIT I
DISCRETE FOURIER TRANSFORMS: Properties of DFT, Linear Filtering methods based on the DFT, Overlap-save, Overlap -Add methods, frequency analysis of signals. Radix-2 FFT and Split- Radix FFT algorithms The Goertzel and Chirp Z transform algorithms

UNIT II

UNIT III
MULTI RATE SIGNAL PROCESSING: Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Filter design & Implementation for sampling rate conversion. Analysis of finite word length effects in fixed-point DSP systems – Fixed, Floating Point arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms

UNIT IV

Text Books:

Reference Books:
M.Tech (Digital Electronics and Communication Systems)
1st semester
AY -2013-14

SYLLABUS
Course Title: ADVANCED OPTIMIZATION TECHNIQUES
Course code: MEP1 1401
L T P C
3 1 0 4

Course objectives:

This course is designed for first year M.Tech students. The course is intended to make the students understand the basic concepts and advanced concepts of optimization techniques.

The main objective of the course is to:

- Develop systematic approach to handle problems to design of electrical circuit etc; with a goal of maximizing the profit and minimizing cost.
- Understand the various optimization techniques such as classified optimization, linear programming. One dimensional minimization methods, unconstrained optimization techniques, constrained optimization techniques and dynamic programming.
- Understand the necessary sufficient conditions for finding the solution of the problems in classical optimization.
- Comprehend the numerical methods for finding approximate solution of complicated problems.
- Apply methods like north-west corner rule, least count method etc. to solve the transportation problem.

Course outcomes:

After undergoing the course, students will be able to

- Design of mechanical systems and interdisciplinary engineering applications and business solutions using suitable optimization technique.
- Apply numerical or iterative techniques in power systems for optimal power flow solutions.
- Optimize the parameters in control systems for desired steady state or transient response.
- Optimize the cost function in deciding economic factors of power systems.
- Design of electrical systems optimally using suitable techniques like univariate method, steepest descent method etc.
UNIT – I:
Linear programming - Two-phase simplex method, Big-M method, duality, interpretation, applications.
Assignment problem - Hungarian’s algorithm, Degeneracy, applications, unbalanced problems, traveling salesman problem.

UNIT – II:
Numerical methods for optimization - Nelder Mead’s Simplex search method, Gradient of a function, Steepest descent method, Newton’s method, types of penalty methods for handling constraints.

UNIT – III:
Genetic algorithm (GA) - Differences and similarities between conventional and evolutionary algorithms, working principle, reproduction, crossover, mutation, termination criteria, different reproduction and crossover operators, GA for constrained optimization, draw backs of GA.
Genetic Programming (GP) - Principles of genetic programming, terminal sets, functional sets, differences between GA & GP, random population generation, solving differential equations using GP.

UNIT – IV:
Multi-Objective GA - Pareto’s analysis, Non-dominated front, multi – objective GA, Nondominated sorted GA, convergence criterion, applications of multi-objective problems.
Basic Problem solving using Genetic algorithm, Genetic Programming & Multi Objective GA and simple applications of optimization for engineering systems.

Text books:
2. Optimization for Engineering Design – Kalyanmoy Deb, PHI Publishers

Reference Books:
2. Genetic Programming- Koza
3. Multi objective Genetic algorithms - Kalyanmoy Deb, PHI Publishers
M.Tech (Digital Electronics and Communication Systems)
1st semester
A Y -2013-14

SYLLABUS

Course Title: Course Code: DIGITAL SYSTEM DESIGN          Course code: ECEP1 1402
L   T      P     C
3   1      0      4

Course objectives

Students undergoing this course are expected to:

- Know digital systems and advantages of digital systems in applications.
- Apply Boolean algebra to switching logic design and simplification.
- Analyze a given digital system and decompose it into logical blocks involving both combinational and sequential circuit elements.
- Understand working of Reduction of state tables and state assignments.
- Learn the Fault Modeling and Test pattern Generation

Course outcomes

After undergoing the course, students will be able to

- Apply knowledge of digital systems, Sequential Circuit Design and design of digital logic circuits
- Know functionality of Sequential circuits and their design
- Explore fault modeling and classes.
- Apply knowledge of kohavi algorithm
- Know functionality of test pattern generation
UNIT – I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT – II


TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT – III


PROGRAMMING LOGIC ARRAYS: Design using PLA’s, PLA minimization and PLA folding.

UNIT – IV

PLA TESTING: Fault models, Test generation and Testable PLA design.

ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

Text Books:

2. Logic Design Theory N. N. Biswas – (PHI)

Reference Books:

Course Title: DETECTION AND ESTIMATION OF SIGNALS (Elective-I) Course Code:ECEP1 1403

Course Objectives:

Students undergoing this course are expected to:

- Learn processing of the analog signal to discrete format in depth
- Understand Curve fitting
- Know the process of Linear filtering
- Understand Spectral analysis of random signals
- Know Detection and estimation of signals.
- Estimate the error from the system using some advanced algorithm.
- Understand Different filtering methods like KF, EKF, and UKF.

Course Outcomes:

After undergoing the course, students will be able to

- Illustrate curve of the data sample even in the noisy environment. This will ensure better estimation with respect to actual data sample.
- visualize the spectral behavior of any practical signal and will be able to estimate many vital statistical analyses (feature analysis) for real time signal processing.
- estimate and detect the instantaneous frequency of the non-stationary signals (radar, speech, biomedical and power) even under noisy condition from the phase angle.
- estimate and detect the presence of radar signal buried in the nose using some advanced algorithm.
- Apply different filtering methods like KF, EKF, and UKF in the applications like Air traffic control, satellite application and estimation of position & velocity in flight.
UNIT I


UNIT II

Detection of signals in noise:- Minimum probability of Error Criterion – Neyman – Person criterion for Radar detection of constant and variable amplitude signals .

UNIT III


UNIT IV
Recursive linear mean squared estimation: - Estimation of a signal parameter. Estimation of time-varying signals – Kalman filtering – Filtering signals in noise Treatment restricted to two variable cases only. Extended and unscented Kalman Filtering.

Text Books:

Reference Books:
3. Introduction to statistical Signal processing with Applications- Srinath, Rajasekaran & Viswanathan, Prentice Hall of India, New Delhi, 110 001,1989.
M.Tech (Digital Electronics and Communication Systems)  
1st semester  
A Y -2013-14

SYLLABUS

Course Title: DIGITAL DESIGN THROUGH VERILOG (Elective-I) Course Code: ECEP 1404

Course Objectives:

Students undergoing this course are expected to:

- Learn the design and implementation of the fundamental digital logic circuits using verilog hardware description language.
- learn the design issues of system on chip.
- understand the system level design and related concepts.
- have awareness on FPGA and CPLD architectures
- implement digital systems on FPGA and CPLD architectures.

Course Outcomes:

After undergoing the course, students will be able to

- Design and implement the fundamental digital logic circuits using verilog HDL.
- Perform system level design.
- Implement design rule checks and timing parameters.
- Demonstrate the architectural details of FPGAs and CPLDs.
- Perform Mini projects on FPGA and CPLD board.

UNIT I

INTRODUCTION TO VERILOG : Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS : Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.
GATE LEVEL MODELING: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

UNIT II
BEHAVIORAL MODELING: Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, Thee ase statement, Simulation Flow. if and if-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

MODELING AT DATA FLOW LEVEL: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

SWITCH LEVEL MODELING.
Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

UNIT III
SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES: Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises,

FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES: Introduction, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines)


UNIT IV
DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE LOGIC DEVICES: Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

VERILOG MODELS: Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design, Design of Microcontroller CPU.

Text books:

Reference Books:
Course Title: VLSI TECHNOLOGY & DESIGN (Elective-I)  
Course Code: ECEP1 1405

Course objectives

Students undergoing this course are expected to:

- make the students understand the basic concepts of VLSI Technology and design of Combinational and Sequential circuits
- explore the concepts of Layout design, Floor planning and Routing.
- Know about the IC fabrication process and technology involved in the production process.
- Comprehend the electrical properties of MOS devices and the relation between physical and electrical parameters of MOS device.
- Know about circuit characterization and performance estimation.
- Understand and to design of Logic Gates using the traditional and alternative logics.
- Analyze the combinational networks and Sequential Networks.
- Learn and explore the issues related to Layout Design, Floor planning and Routing.

Course outcomes

After undergoing this course, students will be able to:

- Identify the issues related to the IC Fabrication Process.
- Explore the design of better devices with IC technology
- Perform circuit characterization and performance estimation.
- Apply the concepts of Logic Gates, Combinational and Sequential networks to design the better.
- Draw better layouts and Optimized floor planning and Routing.
UNIT – I
Review of Microelectronics and introduction to MOS technologies: (MOS, CMOS, Bi CMOS) Technology trends and projections. MOS Fabrication Processes.
Basic Electrical Properties Of MOS, CMOS & BICMOS Circuits: Ids-Vds relationships, Threshold voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II
CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION
Resistance estimation - Capacitance estimation - Inductance - Switching characteristics - Transistor sizing - Power dissipation and design margining - Charge sharing - Scaling.
LOGIC GATES: Static complementary gates, switch logic-pass transistor and transmission gate logic, Alternative gate circuits.

UNIT – III
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.
SEQUENTIAL SYSTEMS: Memory cells and Arrays, clocking disciplines, Design, power optimization, Design validation and testing.

UNIT – IV

Text Books:
1. Essentials of VLSI Circuits and Systems, K. Eshraghian et al PHI of India Ltd.,2005

Reference books:
Course Title: CODING THEORY & PRACTICE (Elective-II)  Course Code: ECEP1 1406

Course objectives

This course enables the students to

- Understand the concepts of information, entropy, mutual information and study the Shannon’s fundamental limits, theorems on information transmission.
- Introduce and classify the Error correcting codes and understand the encoding and decoding of various linear block codes, Convolutional codes.
- Know the mathematical description of error correcting codes.
- Introduce the extension field called Galois field and their role in the design of BCH and RS codes.
- Study the applications of error correcting codes.

Course outcomes

After undergoing this course, students will be able to:

- analyze the information theoretic problems from various disciplines like computer science, mathematics, statistics and communication engineering.
- apply coding techniques in various communication systems like wireless communications to achieve coding gain at low SNR values.
- build new structures for encoder and decoder to address the issues in evaluating performance of communication system.
- solve the problems based on field theory.
- Implement coding techniques in real time systems using FPGA.
UNIT-I
Information Theory: Entropy, Information rate, source coding: Shannon-Fano and Huffman coding techniques, Mutual Information, Channel capacity of Discrete Channel, Shannon- Hartley law, Trade-off between bandwidth and SNR.
Error Control Codes: Examples of the use of error control codes, basic notions, Characterization of Error control codes performance of error control codes, comparison of uncoded and coded systems.

UNIT II
Linear Block Codes: Linear block Codes and their properties, standard arrays, Syndromes, Weight Distribution. Error Detection/Correction Properties, Modified Linear block codes.
Cyclic Codes: General theory, Shift Register Implementations, Shortened Cyclic codes, CRCs for Error Detection.

UNIT III
BCH and RS Codes: Algebraic Description, Frequency Domain Description, Decoding Algorithms for BCH and RS Codes.

UNIT IV
Convolution Codes: Convolution encoders, structural properties of convolution codes, Trellis Diagrams, Viterbi Algorithm, Performance Analysis.
Applications: Concatenated Codes, Interleavers, The Compact Disc, Codes for Magnetic recording.

Text books:

Reference books:
M.Tech (Digital Electronics and Communication Systems)  
1st semester  
A Y -2013-14

SYLLABUS

Course Title: DIGITAL DATA COMMUNICATIONS (Elective-II)  
Course Code: ECEP1 1407

L    T      P     C
3   1      0      4

Course objectives

Students undergoing this course are expected to

- Understand the basics of the communications, and how the data is communicated in terms of digital modulation techniques.
- Learn how to use the digital transmission rather than analog and also multiplexing techniques like TDM, FDM, and WDM.
- Illustrate and explain fundamental architectures of networks and the Internet, as well as their underlying protocols.
- Know different error control codes that is error detection and correction codes.
- Learn the generations of cellular telephone systems and CDMA, GSM, personal communication satellite systems.
- Learn the various wireless local area network architectures and different multimedia systems.

Course outcomes

After undergoing this course, students will be able to

- design, develop and maintain any kind of advanced communication systems.
- develop wireless communication systems and also work with satellite communication systems using different multiplexing techniques like TDM, FDM and WDM.
- acquaint with Data Link Control and Data Link Protocols.
- implement Error Detection and Correction techniques in advanced communication systems
- use the data communication systems and technology in real life applications like defense and research labs.
- understand the application services like wireless LAN.
UNIT I

DIGITAL MODULATION TECHNIQUES: FSK, MSK, BPSK, QPSK, 8-PSK, 16-PSK, 8- QAM, 16- QAM, Band width efficiency carrier recovery, DPSK, clock recovery, Probability of error and bit error rate.

Data Communications: Circuits- Serial, Parallel configuration, Topology, Transmission modes, Two wire verses Four wire operation, Data communication codes- Baudot, ASCII code, EBCDIC code, and Bar code, Error Control – Detection and Correction, synchronization- Character synchronization, LCU.

UNIT II

Serial and Parallel Interfaces , Telephone Networks and Circuits , Data modems- Asynchronous Modems, Synchronous Modems, modem synchronization, Low speed Modems, Medium and High speed Modems, Modem control-The AT command Set, CCITT

Data Communication Protocols, Character and block Mode ,Asynchronous and Synchronous Protocols, public Data Networks, ISDN.

UNIT III

LOCAL AREA NETWORKS : token ring, Ethernet, Traditional, Fast and GIGA bit Ethernet.

DIGITAL MULTIPLEXING : TDM, T1 carrier, CODECS, COMBO CHIPS, North American Hierarchy, Line Encoding, T-carrier, Frame Synchronization Inter Leaving Statistical TDM FDM, Hierarchy, Wave Division Multiplexing.

UNIT IV


MULTI MEDIA: Digitalizing Video and Audio Compression Streaming Stored and Live Video and Audio, Real Time Interactive Video and Audio, VOIP

Text Books:
2. Data communication and networking - B.A. Forouzen, TMH, 3rd edition

Reference Books:
1. Wireless communication and networking - William Stallings, PHI 2003
Course Title: EMBEDDED AND REAL TIME SYSTEMS (Elective-II) Course Code: ECEP1 1408

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Course objectives:

- Design and development of an embedded system, including hardware and embedded software development.
- Understand the basics of an embedded system.
- Program an embedded system with Real-Time aspects.
- Design, implement and test a real time embedded system.
- Learn the difference between real-time and standard operating systems.
- Know the significance of a real time OS in an embedded System.

Course outcomes

After undergoing this course, students will be able to:

- handle many issues involved with embedded systems.
- Understand Real-Time Operating System concepts.
- Program using system calls in ID Environment.
- Program an embedded system with tasks and executive.
- Understand the tools to build an embedded real-time system.
- Design and implement a small embedded system
- Present design information effectively in the forms of technical reports and oral presentations
UNIT I: INTRODUCTION
Embedded systems overview, design challenges, processor technology, Design technology, Trade-offs. Single purpose processors, RT-level combinational logic, sequential logic (RTlevel), custom purpose processor design(RT -level), optimizing custom single purpose processors. General Purpose Processors - Basic architecture, operations, programmer’s view, development environment, Application specific Instruction – Set processors (ASIPs)- Micro controllers and Digital signal processors.

UNIT II: STATE MACHINE AND CONCURRENT PROCESS MODELS AND COMMUNICATION PROCESSES
Introduction, models Vs Languages, finite state machines with data path model (FSMD), program state machine model(PSM, concurrent process model, concurrent processes, communication among processes, synchronization among processes, Implementation, data flow model, real-time systems. Communication Processes - Need for communication interfaces, RS232/UART, RS422/RS485, USB, Infrared, IEEE1394 Firewire, Ethernet, IEEE 802.11, Blue tooth.

UNIT III: INTRODUCTION TO REAL TIME SYSTEMS AND PROGRAMMING LANGUAGES AND TOOLS

UNIT IV: REAL TIME DATABASES AND DESIGN TECHNOLOGY

Text Books:

Reference Books:
Course Title: HDL PROGRAMMING LABORATORY  
Course Code: ECEP1 1209

Course Objectives:

Students undergoing this course are expected to:

- design and implement the fundamental digital logic circuits using verilog hardware description language.
- learn functionality of designed circuits using functional simulator.
- understand the timing and critical issues during simulation.
- synthesize the design.
- learn place and route techniques of different FPGA vendors.

Course Outcomes:

After undergoing the course, students will be able to

- Design and implement the fundamental digital logic circuits using verilog HDL.
- Perform system level design.
- Implement design rule checks and timing parameters.
- know the resources consumed by the design on FPGA.
- Optimize the Interconnections during place and route.

1. Digital Circuits Design (Sub-System Level) Description using Verilog and VHDL.
2. Verification of the Functionality of Designed Circuits using functional Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis Reports of top-order designed Digital circuits.
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices
M. Tech (Digital electronics and communication systems)
2nd semester
A Y -2013-14

SYLLABUS

Course Title: DSP PROCESSORS & ARCHITECTURES
Course Code: ECEP1 1410

Course objectives

Students undergoing this course are expected to:

- understand the basic DFT, FFT and rate conversion algorithms.
- understand the number format, dynamic range and sources of errors in DSP systems.
- learn about TMS programmable DSPs and their programming capabilities.
- Understand basic DSP algorithms on TMS processors.
- Know FFT algorithms on TMS320C54XX DSP device

Course outcomes

After undergoing the course, students will be able to

- Apply DFT and FFT algorithms for DSP application
- Apply the number format, dynamic range and various sources of errors in DSP system
- Implement application programs on a DSP processor
- Implement various DSP algorithms on TMS processors.
- Implement FFT algorithms on TMS320C54XX DSP device
UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), linear time invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT III
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT IV
IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Text books:

Reference Books:
Course Title: SOFT COMPUTING TECHNIQUES
Course Code: CSEP1 1413

Course objectives:
This course is designed for first year M.Tech students. The course is intended to make the students understand concepts about Soft Computing and its application in various field.

The main objective of the course is to

- know Soft Computing basics and its branches
- understand the basic implementation details on Artificial Neural Networks
- understand fuzzy logic and its application in ANN.
- introduction of Support vector machine and its application
- elaborate discussion on applications of Soft Computing

Course outcomes
After undergoing the course, students will be able to

- differentiate between Soft Computing and Hard computing.
- understand its branches Artificial Neural Networks, Fuzzy Logic, and Support Vector machine
- understand various applications of soft computing.
- judge less complexity by using various soft computing methods
UNIT I:
**Basic elements of soft Computing** – Introduction to soft computing, Fuzzy logic, Neural Networks and Evolutionary Computing, Approximations of Multivariate functions, Non – linear Error surface and optimization.

**Artificial Neural Networks**– Introduction, Basic models of ANN, important terminologies, Basic Learning Laws, Supervised Learning Networks, Perceptron Networks, Adaptive Linear Neuron, Backpropagation Network. Radial basis function network and Hopfield Networks.

UNIT II:


UNIT-III :

**Genetic Algorithm**– Introduction, Traditional Optimization and search techniques, Search space, Operators: Encoding, Selection, Crossover and Mutation. Stopping Condition of GA.

UNIT IV:
**Support Vector Machine**– Introduction, optimal hyper plane for linearly separable pattern, linear classifier, nonlinear classifier problem, optimal plane for non-separable pattern, example XOR problem, support vector machine for non-linear regression., summary and discussion.

**Applications of Soft Computing** – A fusion Approach of Multispectral Images with SAR Image for flood area analysis, Optimization of TSP using GA Approach and GA-Fuzzy system for Control of flexible Robots.

**Text Books:**
2. V. Kecman, “Learning and Soft computing”, Pearson Education, India

**Reference Books:**
M.Tech (Digital Electronics and Communication Systems)
2nd semester
A Y -2013-14

SYLLABUS

Course Title: WIRELESS COMMUNICATIONS AND NETWORKS        Course Code: ECEP1 1411

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Course objectives:

Students undergoing this course are expected to:

- Know fundamental concepts of wireless communication systems.
- Understand different multiple access techniques.
- Differentiate wireless and fixed networks.
- Understand various switching techniques and data networks.
- Know the operation of Mobile IP.
- Understand the WAP protocol stack.
- Know the wireless standards like IEEE 802.11,IEEE 802.15.,
- Know Bluetooth radio specifications and protocol architecture.

Course outcomes:

At the end of the course, the students can able to:

- Apply the techniques like frequency reuse, cell splitting, sectoring in wireless systems to improve the coverage and capacity.
- Enhance the existing multiple access techniques to accommodate more users in specified bandwidth.
- Explore the advantages with wireless networks in data communications.
- Propose efficient routing techniques.
- Identify the importance of Mobile IP in wireless systems.
- Compare analogy of WAP with OSI/ISO layer protocols.
- Distinguish various wireless standards like WLAN, Wi-Fi.
- List out the Bluetooth wireless standard protocols.
UNIT I
WIRELESS COMMUNICATIONS & SYSTEM FUNDAMENTALS: Introduction to wireless communications systems, example systems. Cellular concepts-frequency reuse, strategies, interference & system capacity, trunking & grade of service, improving coverage & capacity in cellular systems. Multiple access techniques-FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA, Packet radio access-protocols, capture effect in packet radio, capacity of cellular systems.

UNIT II

UNIT III

UNIT IV
WIRELESS LANS: Infrared LANs, Spread spectrum LANs, Narrow band and microwave LANs, IEEE 802 protocol Architecture, IEEE 802.11 architecture and services, IEEE 802.11 medium access control, IEEE 802.11 physical layer. Bluetooth Overview, Radio specification, Base band specification, Link manager protocol, Logical link control and adaptation protocol.

Text Books:

Reference Books:
M. Tech (Digital electronics and communication systems)
2nd semester
A Y -2013-14

SYLLABUS

Course Title: ANALOG AND DIGITAL IC DESIGN (Elective-III)        Course Code: ECEP1 1412

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3       1      0       4

Course objectives:

Students undergoing this course are expected to:

- Understand the fundamental analog IC blocks
- Understand the basic analog IC blocks like mirrors, references, basic amplifiers and opamps
- Understand the PLL and switched capacitor circuits by using MOSFETS
- Learn VHDL modeling of combinational and sequential circuits
- Learn the internal circuit details of different varieties of ADC and DAC

Course outcomes

At the end of the course, the students can be able to:

- Design and implement the fundamental analog IC blocks
- Demonstrate the internal circuits and topologies of Opamp
- Analyze the PLL and switched capacitors
- Demonstrate the VHDL models for combinational and sequential circuits
- Draw and explain the internal structures of ADC and DAC
UNIT-I
CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: Simple COMS, BJT current mirror, Cascode, Wilson and Widlar current mirrors. Common Source amplifier source follower, common gate amplifier
OPERATIONAL AMPLIFIERS: General considerations one – state op-amps, two stage opamps-gains boosting stage- comparison I/P range limitations slew rate.
PHASED LOCKED LOOP DESIGN: PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs – phase Detector- Voltage controlled oscillator case study.

UNIT -II
COMPARATORS: Using an op-amp for a comparator-charge injection error- latched Comparator
SWITCHED CAPACITORS CIRCUITS: Basic Building blocks op-amps capacitors switches –non-overlapping clocks-Basic operations and analysis-resistor equivalence of la switched capacitor- parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis-First order filters- switch sharing fully differential filters.

UNIT-III
COMBINATIONAL IC DESIGN BY USING VERILOG: VERILOG modeling for decoders, encoders, multiplexers, adders and subtractors.
SEQUENCIAL IC DESIGN BY USING VHD: VERILOG modeling for latches, flip flops, counters, shift registers, FSMs.
LOGIC FAMILIES & CHARACTERISTICS: COMS, TTL, ECL, logic families COMS / TTL- interfacing and comparison of logic families.

UNIT-IV
DIGITAL INTEGRATED SYSTEM BUILDING BLOCKS: Multiplexers, decoders, barrel shifters, counters and digital single bit adders.
NYQUIST RATE D/A CONVERTERS: Decoder based converter resistor storing converters folded resistor string converter – Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.

2. Design of Analog CMOS Integrated Circuits-Bezad Razavi, TMH

Reference Books:
Course Title: RADAR SIGNAL PROCESSING (ELECTIVE-III)  
Course Code: ECEP1 1413

Course Objectives:

Students undergoing this course are expected to

- understand the basic principle of operation of radar and classification of radars
- derive the expression for radar range equation
- understand basic detection of radar signals in noise
- understand the different types of receivers to detect the signal in noise
- know and derive the ambiguity function and its properties
- know the different types radar waveforms
- know the need of pulse compression and understand the different types of pulse compression techniques
- understand different types of nonlinear pulse compression coded waveforms

Course outcomes

At the end of the course, students are able to

- know the operation of CW, FM-CW, MTI and Pulse Doppler radar
- Describe the range ambiguities and various system losses
- know parameters of radar receivers like noise figure, noise temperature
- Design matched filter to detect the signals in noise environment
- derive the ambiguity function
- Design the different types pulse compression coded waveforms
- Describe the application of different waveforms
- Discuss about the design of nonlinear pulse compression waveforms and its advantages
UNIT I

UNIT II

UNIT III

UNIT IV

Text books:

Reference Books:
Course Title: SATELLITE COMMUNICATION SYSTEMS (Elective-III)  Course code: ECEP1 1414

Course Objectives:

Students undergoing this course are expected to

- Understand in-depth knowledge of satellite communication systems operation and planning.
- Know modern satellite multiple access, modulation and coding schemes
- Understand the basics of orbital mechanics, the types of satellite orbits, the location of ground stations, and the look angles from ground stations to the satellite.
- Understanding of link budget equations to provide sufficient margin for performance, that includes examining the various types of modulation, error correcting codes, and encryption.
- Examine concepts of satellite networking, that includes mobile satellite systems for voice and internet communication, data networks, and scientific data.

Course outcomes:

At the end of the course, students are able to

- Specify systems design for satellite communications
- Analyze the performance of satellite communications systems
- Identify the fundamentals of orbital mechanics, the characteristics of common orbits used by Communications and other satellites, and be able to discuss launch methods and technologies
- Calculate an accurate link budget for a satellite or other wireless communications link.
- Describe how analog and digital technologies are used for satellite communications networks and the topologies and applications of those networks, as well as the comparison to alternative communication systems (e.g. – undersea fiber optic cables).
UNIT I

INTRODUCTION:

UNIT II
SATELLITE SUBSYSTEMS:
Attitude and orbit control system, telemetry, tracking, Command and monitoring, power systems, communication subsystems, Satellite antenna Equipment reliability and Space qualification. Satellite link design: Basic transmission theory, system noise temperature and G/T ratio, Design of down links, up link design, Design of satellite links for specified C/N, System design example.

UNIT III
MULTIPLE ACCESS:
Frequency division multiple access (FDMA) Intermodulation, Calculation of C/N. Time division Multiple Access (TDMA) Frame structure, Examples. Satellite Switched TDMA Onboard processing, DAMA, Code Division Multiple access (CDMA), Spread spectrum transmission and reception. Earth station technology: Introduction, Transmitters, Receivers, Antennas, Tracking systems, Terrestrial interface, Primary power test methods.

UNIT IV
LOW EARTH ORBIT AND GEO-STATIONARY SATELLITE SYSTEMS:
Orbit consideration, coverage and frequency considerations, Delay & Throughput considerations, System considerations, Operational NGSO constellation Designs. Satellite navigation & the global positioning system: Radio and Satellite Navigation, GPS Position Location principles, GPS Receivers and codes, Satellite signal acquisition, GPS Navigation Message, GPS signal levels, GPS receiver operation, GPS C/A code accuracy, Differential GPS.

Text Books:

Reference Books:
M.Tech (Digital Electronics and Communication Systems)
2nd semester
A Y -2013-14

SYLLABUS

Course Title: OPTICAL COMMUNICATION AND NETWORKS               Course code:ECEP1 1415
(Elective-IV)

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Course objectives:

Students undergoing this course are expected to

- Understand basics of light waves and their propagation, single/multimode optical fibers.
- Learn the operation of various optical sources and detectors
- Get insight into fabrication methods, optical transmission characteristics, cabling and installation.
- Understand fiber optic networks, Transreceiver, semiconductors optical amplifiers, couplers/splicers, wavelength division multiplexers and demultiplexers, filters, isolators, and optical switches
- Study the design of basic networks and other optical networks.

Course outcomes:

After undergoing the course, students will be able to

- Apply knowledge of mathematics to solve numerical based on step index and graded index fibers pertaining to MSI and MGI, SMSI.
- Analyze the performance of LASERS, LEDs, and Photodiodes.
- Implement fiber cabling and installation.
- Identify the necessity of various components used in optical networks.
- Design various types of optical networks like SONET etc.
Unit – I
Overview of optical fiber communications & Optical Fibers: The evolution of fiber optic systems, elements of an optical fiber transmission link. Advantages of optical fiber communication, applications. Optical Fibers: structures, wave guiding, Nature of light, Basic optical laws and definitions, optical fiber modes and configurations (Fiber types, Rays and modes, step index and graded index fibers). mode theory of circular waveguides.

Unit – II
Optical sources & Photo Detectors: LEDs, structures, quantum efficiency, modulation capability, Laser diodes: Laser diodes and threshold conditions, external quantum efficiency resonant frequencies, laser diode structures and radiation pattern, temperature effects, reliability. Photo Detectors: Physical principles of photodiodes (pin Photodiode, avalanche, photo diode) comparison of photo detectors, noise in detectors.

Unit – III
Optical Communication Systems
Fabrication, cabling and installation: Fabrication, fiber optic cables, Installation- placing the cable. Optical Communication Systems: Block diagrams of optical communication systems, direct intensity modulation, digital communication systems, Laser semiconductor transmitter, Generations of optical fiber link, description of 8 Mb/s optical fiber communication link, description of 2.5 Gb/s optical fiber communication link.

Unit – IV
Components of fiber optic Networks: Overview of fiber optic networks, Transreceiver, semiconductors optical amplifiers, couplers/splicers, wavelength division multiplexers and demultiplexers, filters, isolators and optical switches. Fiber Optic Networks: Basic networks, SONET/SDIT, Broadcast and select WDM Networks, wavelength routed networks, optical CDMA.

Text Books:

Reference Books:
M.Tech (Digital Electronics and Communication Systems)
2nd semester
A Y -2013-14

SYLLABUS

Course Title: SYSTEM MODELLING & SIMULATION (Elective-IV)  Course code: ECEP1 1416

Course objectives:

Students undergoing this course are expected to

- Analyze approaches to system modeling and simulation
- Understand simulation model for linear systems.
- Developing simulation for motion control models.
- Analyze state machine model
- Develop Petri nets for a problem and its analysis
- Understand the simulation of queuing systems
- Know how to optimize the model

Course Outcomes:

- Analyze the given system or problem
- Design a model to represent the system or problem
- Simulate for the designed model
- Develop simulation models for time and event driven systems
- Design simulation models for given system using petri nets
- Analyze the queuing systems
- Optimize the model to get optimum performance
UNIT I - INTRODUCTION TO SIMULATION - 14P

UNIT II - DISCRETE EVENT SIMULATION - 16P
Discrete Event Simulation, Simulation of Single server queuing system, Simulation diagrams, Queing theory, simulating queing systems, Types of Queues, Multiple servers, Simulation of Inventory System.

UNIT III - BUILDING SIMULATION MODELS - 13P
Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation, System identification, Searches, Alpha/beta trackers, multidimensional optimization and modeling and simulation methodology.

UNIT IV - STATE MACHINES MODEING AND SIMULATION - 17P
Disturbance signals, state machines, petri nets & analysis, System encapsulation, Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

Text Books:

Reference Books:
Course Title: VLSI SIGNAL PROCESSING (Elective-IV)  
Course Code: ECEP1 1417

Course objectives:

Students undergoing this course are expected to:

- Understand the pipelining and parallel processing techniques to VLSI systems
- Analyze the retiming, unfolding & folding concepts for register minimization
- Understand the systolic architectures
- Understand the various arithmetic circuits for signal processing
- Understand and apply the fast convolution algorithms for signal processing applications

Course outcomes:

After undergoing the course, students will be able to

- Design parallel processors in VLSI systems
- Implement the register minimization using the retiming, unfolding & folding concepts.
- Design systolic architecture using canonical mapping and generalized mapping
- Design parallel bit circuits
- Implement signal processing applications like FFT etc
UNIT- I
Introduction to the VLSI Signal Processing

Pipelining and parallel processing
Introduction, Data Flow Graph Representation, Loop bound and Iteration Bound, Algorithms for computing Iteration bound, Pipelining of FIR filters, Parallel Processing,

UNIT- II
Retiming
Definitions and Properties, Solving systems of inequalities, Retiming techniques.

Unfolding and Folding

UNIT- III
Systolic Architecture Design

Arithmetic components
Parallel bit circuits: Carry-Look ahead addition, Prefix Computations, Carry-Save Addition, Multiplication.

UNIT- IV
Fast Convolution
Introduction, Cook-Toom algorithm, Winogard algorithm, Iterated Convolution and Cyclic convolution.

Programmable Digital Signal Processors

Text Books:

Reference Books:
Course Title: ADVANCED SIGNAL PROCESSING LABORATORY

Course code: ECEP1 1218

Course objectives:

Students undergoing this course are expected to:

- Understand the basic concept of discrete time signals and their representation in time domain
- Learn the implementation of IIR and FIR filters for the given specifications
- Understand how to improve the quality of an image in spatial domain and Frequency Domain
- Learn about image segmentation using edge detection with the help of derivative operators
- Know the importance of Image Compression using Discrete cosine transform
- Understand the various Morphological Operations on an image

Course outcomes:

After undergoing the course, students will be able to

- Generate the various discrete time signals in time domain
- Design and analyze the IIR and FIR filters for the various specifications
- Enhance the image in spatial domain and Frequency Domain
- Detect the edges of an image using various derivative operators
- Compress the image using various image transforms
- Apply various morphological Operations on an image
The students are required to simulate the following experimental parts on the MATLAB environment by consider the relevant application based examples.

PART-1: Digital Signal Processing

1. Discrete-time Signals in the time domain.
2. z-Transforms and inverse z-Transforms.
3. Properties of Discrete Fourier Transform
4. FIR Filter Design.
5. IIR Filter Design.
6. Adaptive Filtering using LMS algorithm

PART-2: Image Processing

1. Generation of histogram of an image
2. Image Enhancement in spatial domain
3. Image Enhancement in Frequency Domain.
4. Image segmentation using Edge detection
5. Image Compression using DCT
6. Morphological Operations